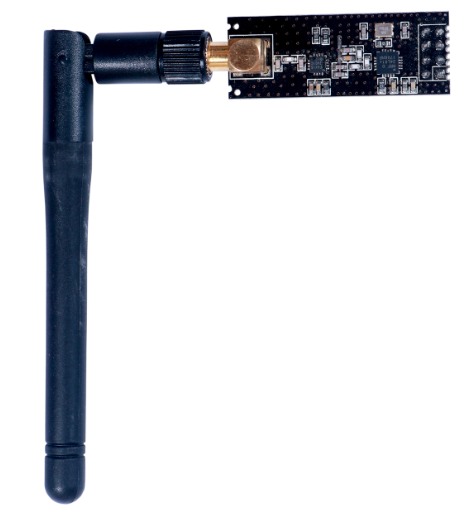
### NRF24L01 2.4GHz Transceiver Module With Antenna



This NRF24L01+PA+LNA Wireless transceiver module is based on 2.4Ghz transceiver NRF24L01+ from Nordic Semiconductors. This board contains a reverse polarized SMA Connector to maximize the RF Range, and there is PA and LNA circuit on board. With the use of external antenna, the range of the device can be very long as compared to a module without this. The antenna is a 2.4 Ghz Antenna with 2 dbi gain. After the use of external antenna, the communication range increases to 800-1000 meters.

The NRF24L01+PA+LNA module is easily attachable to any MCU. This module is designed with power amplifier and SMA Antenna. And that allows it to be used for wireless communication of up to 1000 meters (No Barrier).

**FEATURES:**

* It uses 2.4GHz global open ISM band, with license-free.
* Transmit power is greater than +20 dBm.
* Support six-channel data reception.
* 2Mbit/s speed makes high-quality VoIP possible
* Multi-frequency points: 125 frequency points meet the needs of multi-point communications and frequency hopping.
* Low cost: integrated with high-speed signal processing parts associated with RF protocol, such as: automatically re-send lost packets and generate acknowledge signal;
* SPI interface facilitates the communication with MCU I/O port.
* Facilitate the development for customers, without development RF part.
* Software programming is fully compatible with NRF24L01 modules.

**SPECIFICATIONS:**

**Absolute maximum ratings:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Operating conditions** | **Minimum** | **Maximum** | **Units** |
| Supply voltages | | | |
| VDD | -0.3 | 3.6 | V |
| VSS |  | 0 | V |
| Input voltage | | | |
| VI | -0.3 | 5.25 | V |
| Output voltage | | | |
| VO | VSS to VDD | VSS to VDD |  |
| Total Power Dissipation | | | |
| PD (TA=85°C) |  | 60 | mW |
| Temperatures |  |  |  |
| Operating Temperature | -40 | +85 | °C |
| Storage Temperature | 40 | +125 | °C |

**Operating conditions:**

**ELECTRICAL SPECIFICATIONS**

Conditions: VDD = +3V, VSS = 0V, TA = - 40ºC to + 85ºC

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter (condition)** | **Min.** | **Typ.** | **Max.** | **Units** |
| **Operating condition** | | | | | |
| VDD | Supply voltage | 1.9 | 3.0 | 3.6 | V |
| VDD | Supply voltage if input signals >3.6V | 2.7 | 3.0 | 3.3 | V |
| TEMP | Operating Temperature | -40 | +27 | +85 | ºC |
| **Power consumption** | | | | | |
| **Idle modes** | | | | | |
| IVDD\_PD | Supply current in power down |  | 900 |  | nA |
| IVDD\_ST1 | Supply current in standby-I mode |  | 26 |  | µA |
| IVDD\_ST2 | Supply current in standby-II mode |  | 320 |  | µA |
| IVDD\_SU | Average current during 1.5ms crystal oscillator startup |  | 400 |  | µA |
| **Transmit** | | | | | |
| IVDD\_TX0 | Supply current @ 0dBm output power |  | 11.3 |  | mA |
| IVDD\_TX6 | Supply current @ -6dBm output powe |  | 9.0 |  | mA |
| IVDD\_TX12 | Supply current @ -12dBm output power |  | 7.5 |  | mA |
| IVDD\_TX18 | Supply current @ -18dBm output power |  | 7.0 |  | mA |
| IVDD\_AVG | Average Supply current @ -6dBm output power, ShockBurst™ |  | 0.12 |  | mA |
| IVDD\_TXS | Average current during TX settling |  | 8.0 |  | mA |
| **Receive** | | | | | |
| IVDD\_2M | Supply current 2Mbps |  | 13.5 |  | mA |
| IVDD\_1M | Supply current 1Mbps |  | 13.1 |  | mA |
| IVDD\_250 | Supply current 250kbps |  | 12.6 |  | mA |
| IVDD\_RXS | Average current during RX settling |  | 8.9 |  | mA |
| **General RF conditions** | | | | | |
| fOP | Operating frequency | 2400 |  | 2525 | MHz |
| PLLres | PLL Programming resolution |  | 1 |  | MHz |
| fXTAL | Crystal frequency |  | 16 |  | MHz |
| Δf250 | Frequency deviation @ 250kbps |  | ±160 |  | kHz |
| Δf1M | Frequency deviation @ 1Mbps |  | ±160 |  | kHz |
| Δf2M | Frequency deviation @ 2Mbps |  | ±320 |  | kHz |
| RGFSK | Air Data rate | 250 |  | 2000 | kbps |
| FCHANNEL 1M | Non-overlapping channel spacing @ 250kbps/ 1Mbps |  | 1 |  | MHz |
| FCHANNEL 2M | M Non-overlapping channel spacing @ 2Mbps |  | 2 |  | MHz |
| **Transmitter operation** | | | | | |
| PRF | Maximum Output Power |  | 0 | +4 | dBm |
| PRFC | RF Power Control Range | 16 | 18 | 20 | dB |
| PRFCR | RF Power Accuracy |  |  | ±4 | dB |
| PBW2 | 20dB Bandwidth for Modulated Carrier (2Mbps) |  | 1800 | 2000 | kHz |
| PBW1 | 20dB Bandwidth for Modulated Carrier (1Mbps) |  | 900 | 1000 | kHz |
| PBW250 | 20dB Bandwidth for Modulated Carrier (250kbps) |  | 700 | 800 | kHz |
| PRF1.2 | 1st Adjacent Channel Transmit Power 2MHz (2Mbps) |  |  | -20 | dBc |
| PRF2.2 | 2nd Adjacent Channel Transmit Power 4MHz (2Mbps) |  |  | -50 | dBc |
| PRF1.1 | 1st Adjacent Channel Transmit Power 1MHz (1Mbps) |  |  | -20 | dBc |
| PRF2.1 | 2nd Adjacent Channel Transmit Power 2MHz (1Mbps) |  |  | -45 | dBc |
| PRF1.250 | 1st Adjacent Channel Transmit Power 1MHz (250kbps) |  |  | -30 | dBc |
| PRF2.250 | 2nd Adjacent Channel Transmit Power 2MHz (250kbps) |  |  | -45 | dBc |

**Receiver operation:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Datarate | Symbol | Parameter (condition) | Min. | Typ. | Max. | Unit |
| **RX Sensitivity** | | | | | | |
|  | RXmax | Maximum received signal at <0.1% BER |  | 0 |  | dBm |
| 2Mbps | RXSENS | Sensitivity (0.1%BER) @2Mbps |  | -82 |  | dBm |
| 1Mbps | RXSENS | Sensitivity (0.1%BER) @1Mbps |  | -85 |  | dBm |
| 250kbps | RXSENS | Sensitivity (0.1%BER) @250kbps |  | -94 |  | dBm |
| **RX selectivity according to ETSI EN 300 440-1 V1.3.1 (2001-09)** | | | | | | |
| 2Mbps | C/ICO | C/I Co-channel |  | 7 |  | dBc |
| C/I1ST | 1st ACS (Adjacent Channel Selectivity) C/I 2MHz |  | 3 |  | dBc |
| C/I2ND | 2nd ACS C/I 4MHz |  | -17 |  | dBc |
| C/I3RD | 3rd ACS C/I 6MHz |  | -21 |  | dBc |
| C/INth | Nth ACS C/I, fi > 12MHz |  | -40 |  | dBc |
| C/INth | Nth ACS C/I, fi > 36MHz |  | -48 |  | dBc |
| 1Mbps | C/ICO | C/I Co-channel |  | 9 |  | dBc |
| C/I1ST | 1st ACS C/I 1MHz |  | 8 |  | dBc |
| C/I2ND | D 2nd ACS C/I 2MHz |  | -20 |  | dBc |
| C/I3RD | 3rd ACS C/I 3MHz |  | -30 |  | dBc |
| C/INth | Nth ACS C/I, fi > 6MHz |  | -40 |  | dBc |
| C/INth | Nth ACS C/I, fi > 25MHz |  | -47 |  | dBc |
| 250kbps | C/ICO | C/I Co-channel |  | 12 |  | dBc |
| C/I1ST | 1st ACS C/I 1MHz |  | -12 |  | dBc |
| C/I2ND | 2nd ACS C/I 2MHz |  | -33 |  | dBc |
| C/I3RD | 3rd ACS C/I 3MHz |  | -38 |  | dBc |
| C/INth | Nth ACS C/I, fi > 6MHz |  | -50 |  | dBc |
| C/INth | Nth ACS C/I, fi > 25MHz |  | -60 |  | dBc |
| **RX selectivity with nRF24L01+ equal modulation on interfering signal. Measured using Pin = -67dBm for wanted signal.** | | | | | | |
| 2Mbps | C/ICO | C/I Co-channel (Modulated carrier) |  | 11 |  | dBc |
| C/I1ST | 1st ACS C/I 2MHz |  | 4 |  | dBc |
| C/I2ND | 2nd ACS C/I 4MHz |  | -18 |  | dBc |
| C/I3RD | 3rd ACS C/I 6MHz |  | -24 |  | dBc |
| C/INth | Nth ACS C/I, fi > 12MHz |  | -40 |  | dBc |
| C/INth | Nth ACS C/I, fi > 36MHz |  | -48 |  | dBc |
| 1Mbps | C/ICO | C/I Co-channel |  | 12 |  | dBc |
| C/I1ST | 1st ACS C/I 1MHz |  | 8 |  | dBc |
| C/I2ND | 2nd ACS C/I 2MHz |  | -21 |  | dBc |
| C/I3RD | 3rd ACS C/I 3MHz |  | -30 |  | dBc |
| C/INth | Nth ACS C/I, fi > 6MHz |  | -40 |  | dBc |
| C/INth | Nth ACS C/I, fi > 25MHz |  | -50 |  | dBc |
| 250kbps | C/ICO | C/I Co-channel |  | 7 |  | dBc |
| C/I1ST | 1st ACS C/I 1MHz |  | -12 |  | dBc |
| C/I2ND | 2nd ACS C/I 2MHz |  | -34 |  | dBc |
| C/I3RD | 3rd ACS C/I 3MHz |  | -39 |  | dBc |
| C/INth | Nth ACS C/I, fi >6MHz |  | -50 |  | dBc |
| C/INth | Nth ACS C/I, fi >25MHz |  | -60 |  | dBc |
| **RX intermodulation test performed according to Bluetooth Specification version 2.0** | | | | | | |
| 2Mbps | P\_IM(6) | Input power of IM interferers at 6 and 12MHz offset  from wanted signal |  | -42 |  | dBm |
| P\_IM(8) | Input power of IM interferers at 8 and 16MHz offset  from wanted signal |  | -38 |  | dBm |
| P\_IM(10) | Input power of IM interferers at 10 and 20MHz offset  from wanted signal |  | -37 |  | dBm |
| 1Mbps | P\_IM(3) | Input power of IM interferers at 3 and 6MHz offset  from wanted signal |  | -36 |  | dBm |
| P\_IM(4) | Input power of IM interferers at 4 and 8MHz offset  from wanted signal |  | -36 |  | dBm |
| P\_IM(5) | Input power of IM interferers at 5 and 10MHz offset  from wanted signal |  | -36 |  | dBm |
| 250kbps | P\_IM(3) | Input power of IM interferers at 3 and 6MHz offset  from wanted signal |  | -36 |  | dBm |
| P\_IM(4) | Input power of IM interferers at 4 and 8MHz offset  from wanted signal |  | -36 |  | dBm |
| P\_IM(5) | Input power of IM interferers at 5 and 10MHz offset  from wanted signal |  | -36 |  | dBm |

**Crystal specifications:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter (condition)** | **Min.** | **Typ.** | **Max.** | **Units** |
| Fxo | Crystal Frequency |  | 16 |  | MHz |
| ΔF | Tolerance |  |  | ±60 | ppm |
| C0 | Equivalent parallel capacitance |  | 1.5 | 7.0 | pF |
| Ls | Equivalent serial inductance |  | 30 |  | mH |
| CL | Load capacitance | 8 | 12 | 16 | pF |
| ESR | Equivalent Series Resistance |  |  | 100 | Ω |
| **DC characteristics Digital input pin** | | | | | |
| VIH | HIGH level input voltage | 0.7VDD |  | 5.25a | V |
| VIL | LOW level input voltage | VSS |  | 0.3VDD | V |
| **Digital output pin** | | | | | |
| VOH | HIGH level output voltage (IOH=-0.25mA) | VDD -0.3 |  | VDD | V |
| VOL | LOW level output voltage (IOL=0.25mA) |  |  | 0.3 | V |
| **Power on reset** | | | | | |
| TPUP | Power ramp up time |  |  | 100 | ms |
| TPOR | Power on reset |  |  | 100 | ms |

**FUNCTIONAL BLOCK DIAGRAM :**

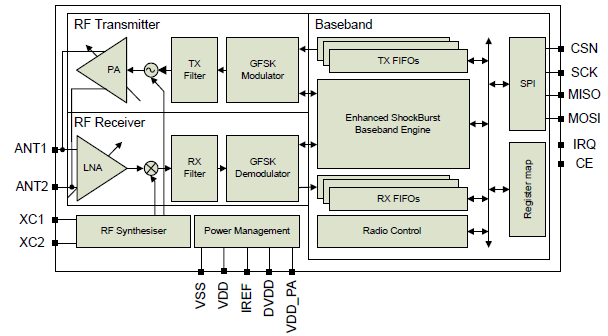


Figure 1. nRF24L01+ block diagram

* The nRF24L01+ is a single chip 2.4GHz transceiver with an embedded baseband protocol engine

(Enhanced ShockBurst™), suitable for ultra low power wireless applications. The nRF24L01+ is designed for operation in the world wide ISM frequency band at 2.400 - 2.4835GHz.

* To design a radio system with the nRF24L01+, you simply need an MCU (microcontroller) and a few external passive components.
* You can operate and configure the nRF24L01+ through a Serial Peripheral Interface (SPI). The register map, which is accessible through the SPI, contains all configuration registers in the nRF24L01+ and is accessible in all operation modes of the chip.
* The embedded baseband protocol engine (Enhanced ShockBurst™) is based on packet communication and supports various modes from manual operation to advanced autonomous protocol operation.
* Internal FIFOs ensure a smooth data flow between the radio front end and the system’s MCU. Enhanced Shock-Burst™ reduces system cost by handling all the high speed link layer operations.
* The radio front end uses GFSK modulation. It has user configurable parameters like frequency channel, output power and air data rate. nRF24L01+ supports an air data rate of 250 kbps, 1 Mbps and 2Mbps.
* The high air data rate combined with two power saving modes make the nRF24L01+ very suitable for ultra low power designs.
* nRF24L01+ is drop-in compatible with nRF24L01 and on-air compatible with nRF2401A, nRF2402, nRF24E1 and nRF24E2. Intermodulation and wideband blocking values in nRF24L01+ are much improved in comparison to the nRF24L01 and the addition of internal filtering to nRF24L01+ has improved the margins for meeting RF regulatory standards. Internal voltage regulators ensure a high Power Supply Rejection Ratio (PSRR) and a wide power supply range.

**FUNCTIONAL DESCRIPTION:**

**STATE DIAGRAM:**

The state diagram in Figure 2. shows the operating modes and how they function. There are three types of distinct states highlighted in the state diagram:

* Recommended operating mode: is a recommended state used during normal operation.
* Possible operating mode: is a possible operating state, but is not used during normal operation.
* Transition state: is a time limited state used during start up of the oscillator and settling of the PLL.

When the VDD reaches 1.9V or higher nRF24L01+ enters the Power on reset state where it remains in reset until entering the Power Down mode.

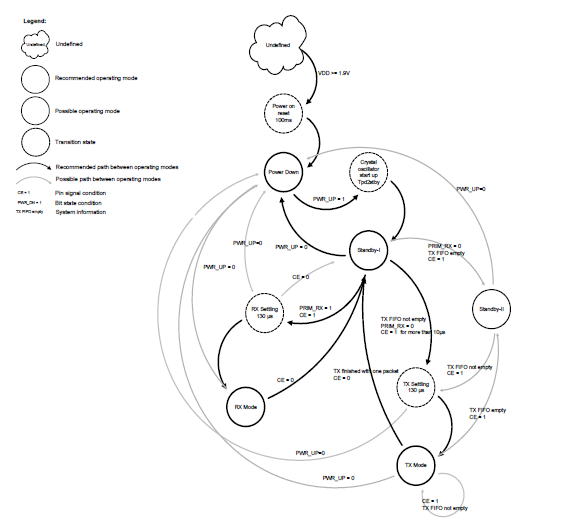


Fig2: Radio control state diagram

**Power Down Mode:**

* In power down mode nRF24L01+ is disabled using minimal current consumption. All register values available are maintained and the SPI is kept active, enabling change of configuration and the uploading/downloading of data registers.
* Power down mode is entered by setting the PWR\_UP bit in the CONFIG register low.

**Standby Modes:**

**Standby-I mode:**

* By setting the PWR\_UP bit in the CONFIG register to 1, the device enters standby-I mode. Standby-I mode is used to minimize average current consumption while maintaining short start up times.
* In this mode only part of the crystal oscillator is active. Change to active modes only happens if CE is set high and when CE is set low, the nRF24L01 returns to standby-I mode from both the TX and RX modes.

**Standby-II mode:**

* In standby-II mode extra clock buffers are active and more current is used compared to standby-I mode. nRF24L01+ enters standby-II mode if CEis held high on a PTX device with an empty TX FIFO. If a new packet is uploaded to the TX FIFO, the PLL immediately starts and the packet is transmitted after the normal PLL settling delay (130μs).
* Register values are maintained and the SPI can be activated during both standby modes.

**RX mode:**

* The RX mode is an active mode where the nRF24L01+ radio is used as a receiver. To enter this mode, the nRF24L01+ must have the PWR\_UP bit, PRIM\_RX bit and the CE pin set high.
* In RX mode the receiver demodulates the signals from the RF channel, constantly presenting the demodulated data to the baseband protocol engine. The baseband protocol engine constantly searches for a valid packet. If a valid packet is found (by a matching address and a valid CRC) the payload of the packet is presented in a vacant slot in the RX FIFOs. If the RX FIFOs are full, the received packet is discarded.
* The nRF24L01+ remains in RX mode until the MCU configures it to standby-I mode or power down mode. However, if the automatic protocol features (Enhanced ShockBurst™) in the baseband protocol engine are enabled, the nRF24L01+ can enter other modes in order to execute the protocol.
* In RX mode a Received Power Detector (RPD) signal is available. The RPD is a signal that is set high when a RF signal higher than -64 dBm is detected inside the receiving frequency channel. The internal RPD signal is filtered before presented to the RPD register. The RF signal must be present for at least 40μs before the RPD is set high.

**TX mode:**

* The TX mode is an active mode for transmitting packets. To enter this mode, the nRF24L01+ must have the PWR\_UP bit set high, PRIM\_RX bit set low, a payload in the TX FIFO and a high pulse on the CE for more than 10μs.
* The nRF24L01+ stays in TX mode until it finishes transmitting a packet. If CE = 0, nRF24L01+ returns to standby-I mode. If CE = 1, the status of the TX FIFO determines the next action. If the TX FIFO is not empty the nRF24L01+ remains in TX mode and transmits the next packet. If the TX FIFO is empty the nRF24L01+ goes into standby-II mode. The nRF24L01+ transmitter PLL operates in open loop when in TX mode. It is important never to keep the nRF24L01+ in TX mode for more than 4ms at a time. If theEnhanced ShockBurst™ features are enabled, nRF24L01+ is never in TX mode longer than 4ms.

**Operational modes configuration:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Mode** | **PWR\_UP**  **register** | **PRIM\_RX**  **register** | **CE input pin** | **FIFO state** |
| RX mode | 1 | 1 | 1 | **-** |
| TX mode | 1 | 0 | 1 | Data in TX FIFOs. Will empty all  levels in TX FIFOsa. |
| TX mode | 1 | 0 | Minimum 10μs  high pulse | Data in TX FIFOs.Will empty one  level in TX FIFOsb. |
| Standby-II | 1 | 0 | 1 | TX FIFO empty. |
| Standby-I | 1 | - | 0 | No ongoing packet transmission. |
| Power Down | 0 | - | - | **-** |

Table 1. nRF24L01+ main modes

* If **CE** is held high all TX FIFOs are emptied and all necessary ACK and possible retransmits are carried

out. The transmission continues as long as the TX FIFO is refilled. If the TX FIFO is empty when

the **CE** is still high, nRF24L01+ enters standby-II mode. In this mode the transmission of a packet is

started as soon as the **CSN** is set high after an upload (UL) of a packet to TX FIFO.

* This operating mode pulses the **CE** high for at least 10μs. This allows one packet to be transmitted.

This is the normal operating mode. After the packet is transmitted, the nRF24L01+ enters standby-I

mode.

**Timing Information**

The timing information in this section relates to the transitions between modes and the timing for the CE

pin. The transition from TX mode to RX mode or vice versa is the same as the transition from the standby

modes to TX mode or RX mode (max. 130μs).

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Name** | **nRF24L01+** | **Max.** | **Min.** | **Comments** |
| Tpd2stby | Power Down → Standby mode | 150μs |  | With external clock |
| 1.5ms |  | External crystal, Ls < 30mH |
| 3ms |  | External crystal, Ls = 60mH |
| 4.5ms |  | External crystal, Ls = 90mH |
| Tstby2a | Standby modes → TX/RX mode |  | 130μs |  |
| Thce | Minimum CE high |  | 10μs |  |
| Tpece2csn | Delay from CE positive edge to CSN  low |  | 4μs |  |

Table2 . Operational timing of nRF24L01+

For nRF24L01+ to go from power down mode to TX or RX mode it must first pass through stand-by mode.

There must be a delay of Tpd2stby (see above Table) after the nRF24L01+ leaves power down mode before the CE is set high.

Note: If VDD is turned off the register value is lost and you must configure nRF24L01+ before entering the TX or RX modes.

**Air data rate:**

* The air data rate is the modulated signaling rate the nRF24L01+ uses when transmitting and receiving data. It can be 250kbps, 1Mbps or 2Mbps. Using lower air data rate gives better receiver sensitivity than higher air data rate. But, high air data rate gives lower average current consumption and reduced probability of on-air collisions.
* The air data rate is set by the RF\_DR bit in the RF\_SETUP register. A transmitter and a receiver must be programmed with the same air data rate to communicate with each other.
* nRF24L01+ is fully compatible with nRF24L01. For compatibility with nRF2401A, nRF2402, nRF24E1, and nRF24E2 the air data rate must be set to 250kbps or 1Mbps.

**RF channel frequency:**

* The RF channel frequency determines the center of the channel used by the nRF24L01+. The channel occupies a bandwidth of less than 1MHz at 250kbps and 1Mbps and a bandwidth of less than 2MHz at 2Mbps. nRF24L01+ can operate on frequencies from 2.400GHz to 2.525GHz. The programming resolution of the RF channel frequency setting is 1MHz.
* At 2Mbps the channel occupies a bandwidth wider than the resolution of the RF channel frequency setting. To ensure non-overlapping channels in 2Mbps mode, the channel spacing must be 2MHz or more.
* At 1Mbps and 250kbps the channel bandwidth is the same or lower than the resolution of the RF frequency.
* The RF channel frequency is set by the RF\_CH register according to the following formula:

F0= 2400 + RF\_CH [MHz]

* You must program a transmitter and a receiver with the same RF channel frequency to communicate with each other.

**Received Power Detector measurements:**

* Received Power Detector (RPD), located in register 09, bit 0, triggers at received power levels above -64 dBm that are present in the RF channel you receive on. If the received power is less than -64 dBm, RDP = 0.
* The RPD can be read out at any time while nRF24L01+ is in receive mode. This offers a snapshot of the current received power level in the channel. The RPD status is latched when a valid packet is received which then indicates signal strength from your own transmitter. If no packets are received the RPD is latched at the end of a receive period as a result of host MCU setting CE low or RX time out controlled by Enhanced ShockBurst™.
* The status of RPD is correct when RX mode is enabled and after a wait time of Tstby2a +Tdelay\_AGC= 130us + 40us. The RX gain varies over temperature which means that the RPD threshold also varies over temperature. The RPD threshold value is reduced by - 5dB at T = -40°C and increased by + 5dB at 85°C.

**PA control:**

The PA (Power Amplifier) control is used to set the output power from the nRF24L01+ power amplifier. The PA control is set by the RF\_PWR bits in the RF\_SETUP register.

|  |  |  |
| --- | --- | --- |
| **SPI RF-SETUP**  **(RF\_PWR)** | **RF output power** | **DC current**  **consumption** |
| **11** | 0dBm | 11.3mA |
| **10** | -6dBm | 9.0mA |
| **01** | -12dBm | 7.5mA |
| **00** | -18dBm | 7.0mA |

Table 3. RF output power setting for the nRF24L01+

Conditions: VDD = 3.0V, VSS= 0V, TA = 27ºC, Load impedance = 15Ω+j88Ω.

**RX/TX control:**

The RX/TX control is set by PRIM\_RX bit in the CONFIG register and sets the nRF24L01+ in transmit/receive mode.

**Enhanced ShockBurst™:**

* Enhanced ShockBurst™ is a packet based data link layer that features automatic packet assembly and timing, automatic acknowledgement and retransmissions of packets. Enhanced ShockBurst™ enables the implementation of ultra low power and high performance communication with low cost host microcontrollers.
* The Enhanced ShockBurst™ features enable significant improvements of power efficiency for bidirectional and uni-directional systems, without adding complexity on the host controller side.
* Enhanced ShockBurst™ features automatic packet transaction handling for the easy implementation of a reliable bi-directional data link. An Enhanced ShockBurst™ packet transaction is a packet exchange between two transceivers, with one transceiver acting as the Primary Receiver (PRX) and the other transceiver acting as the Primary Transmitter (PTX).
* An Enhanced ShockBurst™ packet transaction is always initiated by a packet transmission from the PTX, the transaction is complete when the PTX has received an acknowledgment packet (ACK packet) from the PRX. The PRX can attach user data to the ACK packet enabling a bi-directional data link.

The automatic packet transaction handling works as follows:

1. You begin the transaction by transmitting a data packet from the PTX to the PRX. Enhanced

ShockBurst™ automatically sets the PTX in receive mode to wait for the ACK packet.

2. If the packet is received by the PRX, Enhanced ShockBurst™ automatically assembles and

transmits an acknowledgment packet (ACK packet) to the PTX before returning to receive mode.

3. If the PTX does not receive the ACK packet immediately, Enhanced ShockBurst™ automatically

retransmits the original data packet after a programmable delay and sets the PTX in receive mode to wait for the ACK packet.

* In Enhanced ShockBurst™ it is possible to configure parameters such as the maximum number of retransmits and the delay from one transmission to the next retransmission. All automatic handling is done without the involvement of the MCU.

**Data and Control Interface:**

The data and control interface gives you access to all the features in the nRF24L01+. The data and control

interface consists of the following six 5Volt tolerant digital signals:

* IRQ (this signal is active low and controlled by three maskable interrupt sources)
* CE (this signal is active high and used to activate the chip in RX or TX mode)
* CSN (SPI signal)
* SCK (SPI signal)
* MOSI (SPI signal)
* MISO (SPI signal)

Using 1 byte SPI commands, you can activate the nRF24L01+ data FIFOs or the register map during all

modes of operation.

**FEATURES:**

* Special SPI commands for quick access to the most frequently used features
* 0-10Mbps 4-wire SPI
* 8 bit command set
* Easily configurable register map
* Full three level FIFO for both TX and RX direction

**Functional description:**

The SPI is a standard SPI with a maximum data rate of 10Mbps.

**SPI operation:**

This section describes the SPI commands and timing.

**SPI commands**

* The SPI commands are shown in Table 20. Every new command must be started by a high to low transition on CSN.
* The STATUS register is serially shifted out on the MISO pin simultaneously to the SPI command word shifting to the MOSI pin.
* The serial shifting SPI commands is in the following format:

<**Command word**: MSBit to LSBit (one byte)>

<**Data bytes**: LSByte to MSByte, MSBit in each byte first>

|  |  |  |  |
| --- | --- | --- | --- |
| **Command name** | **Command**  **word (binary)** | **# Data bytes** | **Operation** |
| R\_REGISTER | 000A AAAA | 1 to 5  LSByte first | Read command and status registers. AAAAA =  5 bit Register Map Address |
| W\_REGISTER | 001A AAAA | 1 to 5  LSByte first | Write command and status registers. AAAAA = 5  bit Register Map Address  Executable in power down or standby modes  only. |
| R\_RX\_PAYLOAD | 0110 0001 | 1 to 32  LSByte first | Read RX-payload: 1 – 32 bytes. A read operation  always starts at byte 0. Payload is deleted from  FIFO after it is read. Used in RX mode. |
| W\_TX\_PAYLOAD | 1010 0000 | 1 to 32  LSByte first | Write TX-payload: 1 – 32 bytes. A write operation  always starts at byte 0 used in TX payload. |
| FLUSH\_TX | 1110 0001 | 0 | Flush TX FIFO, used in TX mode |
| FLUSH\_RX | 1110 0010 | 0 | Flush RX FIFO, used in RX mode  Should not be executed during transmission of  acknowledge, that is, acknowledge package will  not be completed. |
| REUSE\_TX\_PL | 1110 0011 | 0 | Used for a PTX device  Reuse last transmitted payload.  TX payload reuse is active until  W\_TX\_PAYLOAD or FLUSH TX is executed. TX  payload reuse must not be activated or deactivated  during package transmission. |
| R\_RX\_PL\_WIDa | 0110 0000 | 1 | Read RX payload width for the top  R\_RX\_PAYLOAD in the RX FIFO.  **Note:** Flush RX FIFO if the read value is larger  than 32 bytes. |
| W\_ACK\_PAYLOADa | 1010 1PPP | 1 to 32  LSByte first | Used in RX mode.  Write Payload to be transmitted together with  ACK packet on PIPE PPP. (PPP valid in the  range from 000 to 101). Maximum three ACK  packet payloads can be pending. Payloads with  same PPP are handled using first in - first out  principle. Write payload: 1– 32 bytes. A write  operation always starts at byte 0. |
| W\_TX\_PAYLOAD\_NO  ACKa | 1011 0000 | 1 to 32  LSByte first | Used in TX mode. Disables AUTOACK on this  specific packet. |
| NOP | 1111 1111 | 0 | No Operation. Might be used to read the STATUS  register |

Table 4. Command set for the nRF24L01+ SPI

The W\_REGISTER and R\_REGISTER commands operate on single or multi-byte registers. When accessing multi-byte registers read or write to the MSBit of LSByte first. You can terminate the writing before all bytes in a multi-byte register are written, leaving the unwritten MSByte(s) unchanged. For example, the LSByte of RX\_ADDR\_P0 can be modified by writing only one byte to the RX\_ADDR\_P0 register. The content of the status register is always read to MISO after a high to low transition on CSN.

Note: The 3 bit pipe information in the STATUS register is updated during the IRQ pin high to low transition. The pipe information is unreliable if the STATUS register is read during an IRQ pin high to low transition.

**SPI timing:**

SPI operation and timing is shown in Fig. nRF24L01+ must be in a standby or power down mode before writing to the configuration registers.

In Figure 3. to Figure 4 the following abbreviations are used:

|  |  |
| --- | --- |
| **Abbreviation** | **Description** |
| Cn | SPI command bit |
| Sn | STATUS register bit |
| Dn | Data Bit (**Note:** LSByte to MSByte, MSBit in each byte first) |

Table 5. Abbreviations used in Figure 3. to Figure 4.

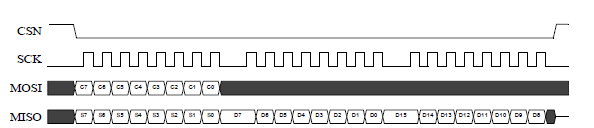


Figure 3. SPI read operation

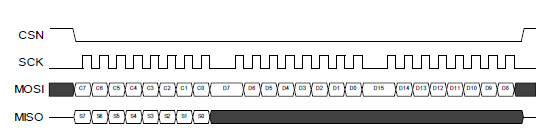


Figure 4. SPI write operation

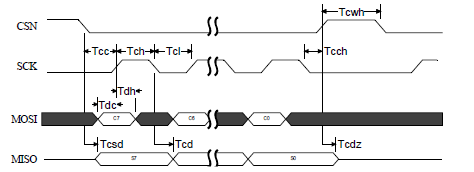


Figure 5. SPI NOP timing diagram

**Peripheral RF Information:**

**Antenna output:**

The ANT1 and ANT2 output pins provide a balanced RF output to the antenna. The pins must have a DCpath to VDD\_PA, either through a RF choke or through the center point in a balanced dipole antenna. A load of 15Ω+j88Ω is recommended for maximum output power (0dBm). Lower load impedance (for instance, 50Ω) can be obtained by fitting a simple matching network between the load and ANT1 andANT2.

**Crystal oscillator:**

* To achieve a crystal oscillator solution with low power consumption and fast start up time use a crystal with a low load capacitance specification. A lower C0 also gives lower current consumption and faster start up time, but can increase the cost of the crystal. Typically C0=1.5pF at a crystal specified for C0max=7.0pF.
* The crystal load capacitance, CL, is given by:

where C1’ = C1 + CPCB1 +CI1 and C2’ = C2 + CPCB2 + CI2

C1 and C2 are SMD capacitors. CPCB1 and CPCB2 are the layout parasitic on the circuit board. CI1 and CI2 are the internal capacitance load of the **XC1** and **XC2** pins respectively; the value is typically 1pF for both these pins.

**Crystal parameters:**

The MCU sets the requirement of load capacitance CL when it is driving the nRF24L01+ clock input. A frequency

accuracy of ±60ppm is required to get a functional radio link. The nRF24L01+ loads the crystal by

1pF in addition to the PCB routing.

**Input crystal amplitude and current consumption:**

The input signal should not have amplitudes exceeding any rail voltage. Exceeding rail voltage excites the

ESD structure and consequently, the radio performance degrades below specification. You must use an

external DC block if you are testing the nRF24L01+ with a reference source that has no DC offset (which is

usual with a RF source).

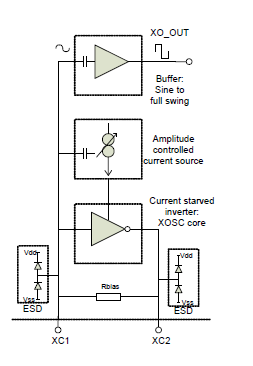
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Figure 6. Principle of crystal oscillator

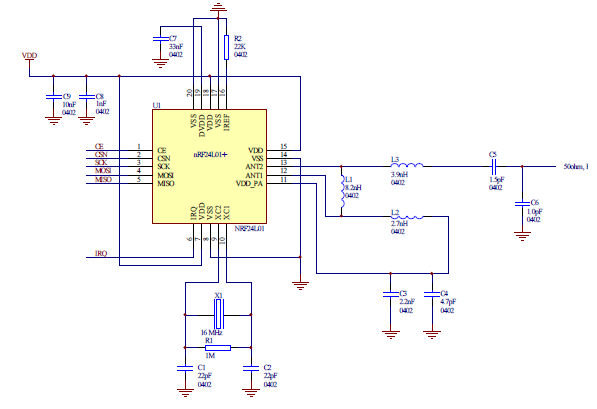
The nRF24L01+ crystal oscillator is amplitude regulated. It is recommended to use an input signal larger than 0.4V-peak to achieve low current consumption and good signal-to-noise ratio when using an external clock. **XC2** is not used and can be left as an open pin when clocked externally.

**PIN FUNCTION:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Pin No** | **Pin Name** | **Pin function** | **Description** |
| 1 | CE | Digital Input | Chip Enable Activates RX or TX mode |
| 2 | CSN | Digital Input | SPI Chip Select |
| 3 | SCK | Digital Input | SPI Clock |
| 4 | MOSI | Digital Input | SPI Slave Data Input |
| 5 | MISO | Digital Output | SPI Slave Data Output, with tri-state option |
| 6 | IRQ | Digital Output | Maskable interrupt pin Active low |
| 7 | VDD | Power | Power Supply (+1.9V - +3.6V DC) |
| 8 | VSS | Power | Ground (0V) |
| 9 | XC2 | Analog Output | Crystal Pin 2 |
| 10 | XC1 | Analog Input | Crystal Pin 1 |
| 11 | VDD\_PA | Power Output | Power Supply Output (+1.8V) for the internal  nRF24L01+ Power Amplifier. |
| 12 | ANT1 | RF | Antenna interface 1 |
| 13 | ANT2 | RF | Antenna interface 2 |
| 14 | VSS | Power | Ground (0V) |
| 15 | VDD | Power | Power Supply (+1.9V - +3.6V DC) |
| 16 | IREF | Analog Input | Reference current |
| 17 | VSS | Power | Ground (0V) |
| 18 | VDD | Power | Power Supply (+1.9V - +3.6V DC) |
| 19 | DVDD | Power Output | Internal digital supply output for de-coupling purposes. |
| 20 | VSS | Power | Ground (0V) |

**TYPICAL APPLICATION CIRCUIT:**

nRF24L01 with single ended matching network crystal, bias resistor, and decoupling capacitors.



**APPLICATIONS:**

* Wireless mouse, keyboard, joystick
* Keyless entry
* Wireless data communication
* Alarm and security systems
* Home automation
* Automotive
* Surveillance
* Telemetry
* Intelligent sports equipment
* Industrial sensors
* Toys

**PACKAGE INCLUDES:**

* 1 x 2.4 Ghz NRF24L01+PA+LNA Module
* 1 x SMA Antenna